# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re Application of: | ) |
| | ) Atty. Docket: **KUBOTA 0007** |
| FURUSHO, Shinji | ) |
| | ) |
| Serial No. _____ (corres. to Int'l. | ) |
| Apln. PCT/JP00/05947 filed 1 September | ) |
| 2000) | ) |
| | ) |
| Filed: Herewith | ) |
| | ) |
| For:    PARALLEL COMPUTER | ) |
|          ARCHITECTURE, AND | ) |
|          INFORMATION PROCESSING | ) |
|          UNIT USING THE | ) Date:  14 March 2002 |
|          ARCHITECTURE | ) |

## PRELIMINARY AMENDMENT (A)

**BOX:  PCT – DO/EO/US**
Assistant Commissioner for Patents
Washington, D. C.  20231

Sir:

Prior to calculating the filing fees, kindly amend the above-captioned

application as follows:

## IN THE CLAIMS:

Kindly amend claims 3, 7 and 8 to read as follows:

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3.       (Amended)  The computer architecture according to claim 1, wherein

each of said memory modules receives a synchronization signal for achieving

synchronization with the CPU module and other memory modules, and

it is constituted such that it comprises input that is connectable to any of said plurality

of sets of buses, and output that is connectable to any other of said plurality of sets of

buses, and at least, it is able to output data according to said synchronization signal by